REMARKS

Applicant respectfully requests reconsideration of the present application.

Office Action Rejections Summary

Claims 1-4, 6-16, and 18-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cideciyan (US 5,177,482).

Claim 21 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Cideciyan in view of Matsui (US 5,825,309) or Millman, "Microelectronics Digital and Analog Circuits and Systems."

Status of Claims

Claims 1-4, 6-16, and 18-21 were pending. Claim 10 has been canceled without prejudice. Claims 8 and 11 have been amended without introducing any new matter. Claims 1-4, 6-9, 11-16, and 18-21 remain pending.

Claim Rejections

The Examiner has rejected claims 1-4, 6-16, and 18-20 under 35 U.S.C. § 103(a) as being unpatentable over Cideciyan (US 5,177,482). Claim 10 has been canceled without prejudice, thus obviating the rejection. Applicant respectfully traverses the rejection on claims 1-4, 6-9, 11-16, and 18-20.

Claim 1 sets forth:

> evaluating one or more source characters to determine an ***intermediate*** running disparity for each of the one or more source characters; and
>
> determining a running disparity for each of the one or more source characters before encoding the one or more source characters based on a current running disparity associated with the one or more source characters and the intermediate running disparity of each of the one or more source characters.

(Claim 1; emphasis added)

In contrast, Cideciyan discloses a patentably distinct encoding scheme. Cideciyan discloses a state transition bit T and a coder state bit S. The next coder state bit S(N+1) is generated from an old coder state bit S(N) and an old state transition bit T(N) as follows:

$$S(N+1) = S(N) \text{ XOR } T(N)$$

(Cideciyan, col. 7, ln. 39-41; col. 11, ln. 28-32 and 61-66; Figures 2 and 8). According to Cideciyan, T(N) is a function of the old data byte, DB(N) (Cideciyan, col. 7, ln. 39-41; Figure 2). Thus, S(N+1) is derived from S(N) and DB(N). The Examiner analogized S to be the running disparity in the current application, T to be the flip/hold bit in the current application, and DB to be the source character in the current application. Applying the Examiner's analogy, the running disparity S(N+1) of a source character DB(N+1) is derived from a current running disparity S(N) and a

current source character DB(N) associated with S(N). However, this is contrary to claim 1, which sets forth determining a running disparity for each of the one or more source characters based on a current running disparity associated with the one or more source characters and the ***intermediate running disparity*** of each of the one or more source characters. The intermediate running disparity of each of the one or more source characters is determined by evaluating ***the one or more source characters***. For example, as illustrated in Figure 7 of the current application, the running disparity RD 780 of Input4 (an example of source characters) is derived from the current running disparity from register D 740 and a corresponding intermediate running disparity ID 774, which is derived from Input 4 and ID 772, which is derived Input3 and ID 770, which is derived from Input 2 and Input 1.

Referring back to Cideciyan, the coder state bit, which was analogized to be the running disparity, is derived by:

$$S(N+1) = S(N) \text{ XOR } T(N),$$

where T(N) = f(D(N)). Cideciyan fails to disclose an ***intermediate*** running disparity. However, the Examiner referred to column 11, lines 61-67 in Cideciyan and alleged that the passage disclosed the intermediate running disparity. It is respectfully submitted that the aforementioned passage merely discloses that S(N+q) = S(N+q-1) XOR T(N+q-1). Again, the coder state bit S(N+q) is derived from a current coder state S(N+q-1) and a current state transition bit T(N+q-1). S(N+q) is not based on any

intermediate running disparity. Although S(N+q) may be derived in advance per Cideciyan, it is not an "intermediate" coder state bit for the corresponding data byte DB(N+q). Rather, S(N+q) ***is*** the coder state bit of DB(N+q).

Note that the Examiner analogized T(N) to be the flip/hold (F/H) bit recited in some of the claims (e.g., claim 2) in the final Office Action (Final Office Action mailed 3/13/06, p. 2). As discussed above, the intermediate running disparity as claimed is a distinct parameter from the F/H bit. Therefore, to be consistent with the Examiner's analogy in the final Office Action, T(N) cannot be the intermediate running disparity as claimed.

For at least the above reasons, claim 1 is patentable over Cideciyan. Withdrawal of the rejection is respectfully requested.

Claim 8 as amended sets forth:

> a pre-calculator to determine an intermediate running disparity for each of the plurality of source characters; and
>
> a comparator coupled to the decoder and the pre-calculator to compare the ***intermediate running disparity*** of each of the plurality of source characters with the current running disparity to determine a running disparity for the respective source character before the respective source character is encoded.

(Claim 8, emphasis added).

In contrast, Cideciyan discloses a patentably distinct encoding scheme. Cideciyan discloses a state transition bit T and a coder state bit S. The next coder state bit S(N+1) is generated from an old coder state bit S(N) and an old state transition bit T(N) as follows:

$$S(N+1) = S(N) \text{ XOR } T(N)$$

(Cideciyan, col. 7, ln. 39-41; col. 11, ln. 28-32 and 61-66; Figures 2 and 8). According to Cideciyan, T(N) is a function of the old data byte, DB(N) (Cideciyan, col. 7, ln. 39-41; Figure 2). Thus, S(N+1) is derived from S(N) and DB(N). The Examiner analogized S to be the running disparity in the current application, T to be the flip/hold bit in the current application, and DB to be the source character in the current application. Applying the Examiner's analogy, the running disparity S(N+1) of a source character DB(N+1) is derived from a current running disparity S(N) and a ***current source character DB(N)*** associated with S(N). However, this is contrary to claim 1, which sets forth determining a running disparity for each of the one or more source characters based on a current running disparity associated with the one or more source characters and the ***intermediate running disparity*** of each of the one or more source characters. The intermediate running disparity of each of the one or more source characters is determined by evaluating ***the one or more source characters***. For example, as illustrated in Figure 7 of the current application, the running disparity RD 780 of Input4 (an example of source characters) is derived

from the current running disparity from register D 740 and a corresponding intermediate running disparity ID 774, which is derived from Input 4 and ID 772, which is derived Input3 and ID 770, which is derived from Input 2 and Input 1.

Referring back to Cideciyan, the coder state bit, which was analogized to be the running disparity, is derived by:

$$S(N+1) = S(N) \text{ XOR } T(N),$$

where T(N) = f(D(N)). Cideciyan fails to disclose an ***intermediate*** running disparity. However, the Examiner referred to column 11, lines 61-67 in Cideciyan and alleged that the passage disclosed the intermediate running disparity. It is respectfully submitted that the aforementioned passage merely discloses that S(N+q) = S(N+q-1) XOR T(N+q-1). Again, the coder state bit S(N+q) is derived from a current coder state S(N+q-1) and a current state transition bit T(N+q-1). S(N+q) is not based on any intermediate running disparity. Although S(N+q) may be derived in advance per Cideciyan, it is not an "intermediate" coder state bit for the corresponding data byte DB(N+q). Rather, S(N+q) ***is*** the coder state bit of DB(N+q).

Therefore, claim 8 is patentable over Cideciyan for at least this reason. Applicant respectfully requests withdrawal of the rejection.

Claim 14 is patentable over Cideciyan in view of Matsui or Millman for at least the reason discussed above with respect to claim 1. Withdrawal of the rejection is respectfully requested.

Claims 2-4, 6-7, 9-13, 15-16, and 18-20 depend, directly or indirectly, from claims 1, 8, and 14, respectively. For at least the reasons discussed above with respect to claims 1, 8, and 14, respectively, claims 2-4, 6-7, 9-13, 15-16, and 18-20 are patentable over Cideciyan. Applicant respectfully requests the Examiner to withdraw the rejection.

Claim 21 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Cideciyan in view of Matsui (US 5,825,309) or Millman, "Microelectronics Digital and Analog Circuits and Systems." Applicant respectfully traverses the rejection. Claim 21 depends from claim 1 and includes all limitations of claim 1. For the reason discussed above with respect to claim 1, Cideciyan does not teach all limitations of claim 14. Furthermore, neither Matsui nor Millman makes up the deficiencies of Cideciyan. Matsui and Millman merely disclose the use of lookup tables. Therefore, a combination of Cideciyan and Matsui or Cideciyan and Millman does not include all the limitations in claim 14. Thus, claim 14 is patentable over Cideciyan in view of Matsui or Millman for at least this reason. Applicant respectfully requests withdrawal of the rejection

Conclusion

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call C. Teresa Wong at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), Applicant hereby requests and authorizes the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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